10A, 30V, 0.200 Ohm, Logic Level, P-Channel Power MOSFET

These products are P-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49205.

Ordering Information

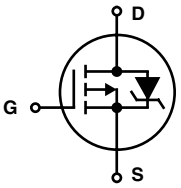
PART NUMBER	PACKAGE	BRAND
RFD10P03L	TO-251AA	10P03L
RFD10P03LSM	TO-252AA	10P03L
RFP10P03L	TO-220AB	F10P03L

NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-252AA variant in tape and reel, i.e. RFD10P03LSM9A..

Features

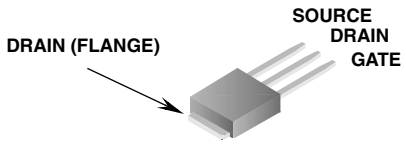
- 10A, 30V
- $r_{DS(ON)} = 0.200\Omega$
- Temperature Compensating PSPICE® Model
- PSPICE Thermal Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature

Symbol

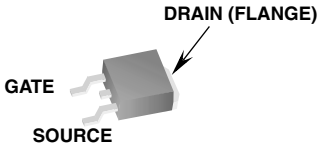


Packaging

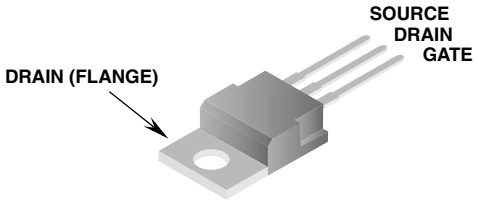
JEDEC TO-251AA



JEDEC TO-252AA



JEDEC TO-220AB



Absolute Maximum Ratings $T_C = 25^oC$ Unless Otherwise Specifie

	RFD10P03L, RFD10P03LSM, RFP10P03L	UNITS
Drain to Source Voltage . . . . . V_{DSS}	-30	V
Drain to Gate Voltage (R_{GS} = 20KΩ) . . . . . V_{DGR}	-30	V
Gate to Source Voltage . . . . . V_{GS}	±10	V
Drain Current		
RMS Continuous . . . . . I_D	10	A
Pulsed Drain Current . . . . . I_{DM}	See Figure 5	
Single Pulse Avalanche Rating . . . . . E_{AS}	Refer to UIS Curve	
Power Dissipation . . . . . P_D	65	W
Derate Above 25^oC	0.43	$W/^oC$
Operating and Storage Temperature . . . . . T_J, T_{STG}	-55 to 175	^oC
Maximum Lead Temperature for Soldering . . . . . T_L (0.063in (1.6mm) from case for 10s)	300	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 11)		-30	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA (Figure 12)		-1	-	-2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30V,	$T_C = 25^oC$	-	-	-1	μA
		V_{GS} = 0V	$T_C = 150^oC$	-	-	-50	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±10V		-	-	±100	nA
Drain to Source On Resistance (Note 1)	$r_{DS(ON)}$	I_D = 10A, V_{GS} = -5V (Figures 9, 10)		-	-	0.200	Ω
		I_D = 10A, V_{GS} = -4.5V (Figures 9, 10)				0.220	Ω
Turn-On Time	t_{ON}	V_{DD} = 15V, $I_D \cong$ 10A, R_L = 1.5Ω, R_{GS} = 5Ω, V_{GS} = -5V (Figure 13)		-	-	100	ns
Turn-On Delay Time	$t_{d(ON)}$			-	15	-	ns
Rise Time	t_r			-	50	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	35	-	ns
Fall Time	t_f			-	20	-	ns
Turn-Off Time	t_{OFF}			-	-	80	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0 to -10V	V_{DD} = -24V, $I_D \cong$ 10A, R_L = 2.4Ω $I_{g(REF)}$ = -0.25mA (Figure 14)	-	25	30	nC
Gate Charge at -5V	$Q_{g(-5)}$	V_{GS} = 0 to -5V		-	13	16	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0 to -1V		-	1.2	1.5	nC
Input Capacitance	C_{ISS}	V_{DS} = -25V, V_{GS} = 0V, f = 1MHz (Figure 15)		-	1035	-	pF
Output Capacitance	C_{OSS}			-	340	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	35	-	pF
Thermal Resistance, Junction to Case	$R_{\theta JC}$			-	-	2.30	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	RFD10P03L, RFD10P03LSM		-	-	100	$^oC/W$
		RFP10P03L				80	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Forward Voltage	V_{SD}	I_{SD} = -10A	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = -10A, dI_{SD}/dt = -100A/μs	-	-	75	ns

NOTE:

2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

Typical Performance Curves Unless Otherwise Specified

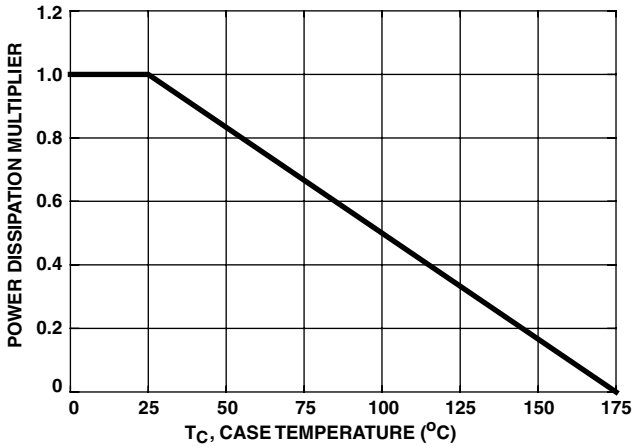


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

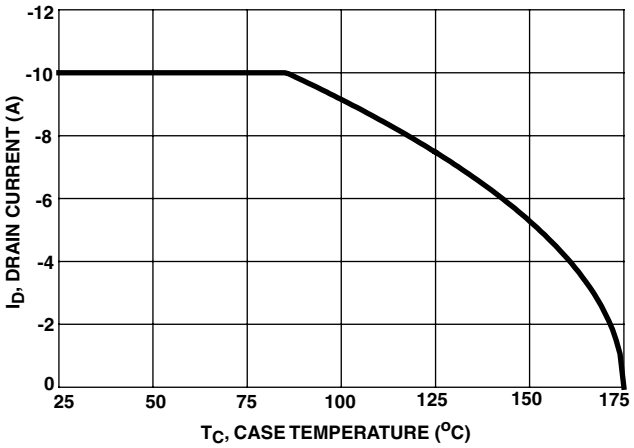


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

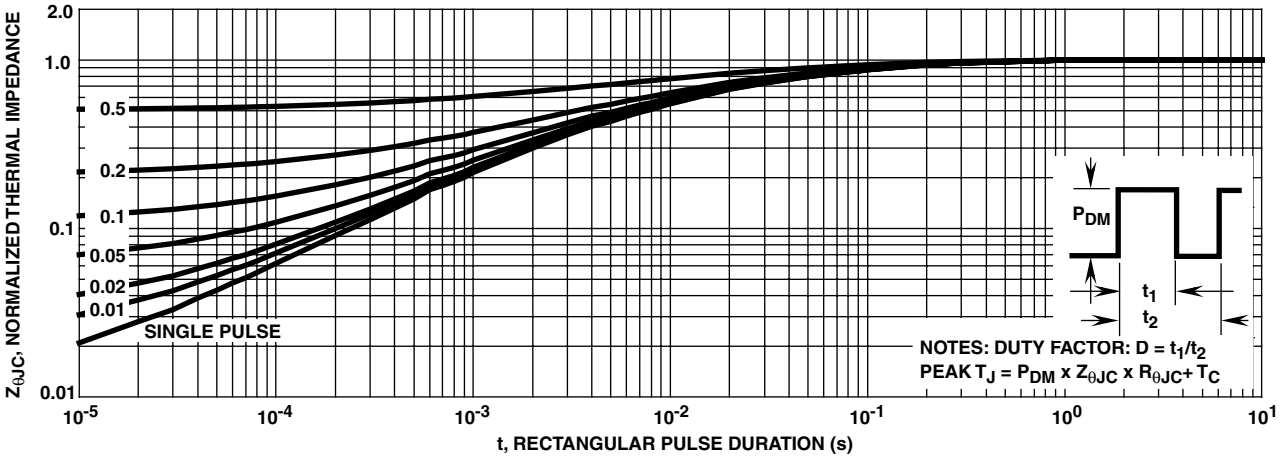


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

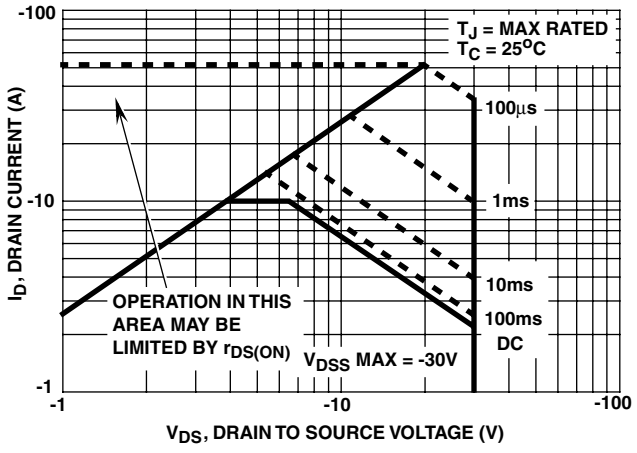


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

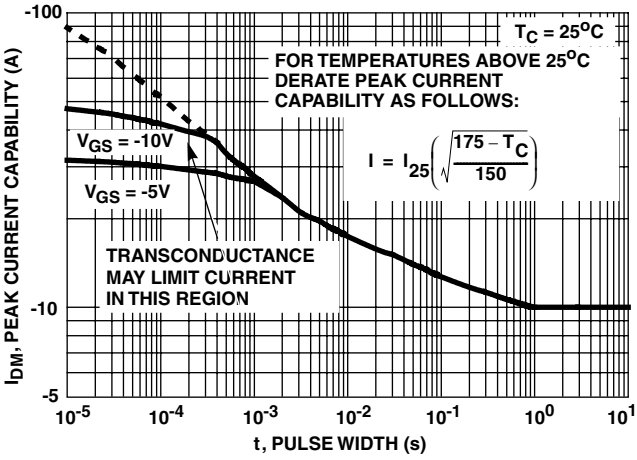
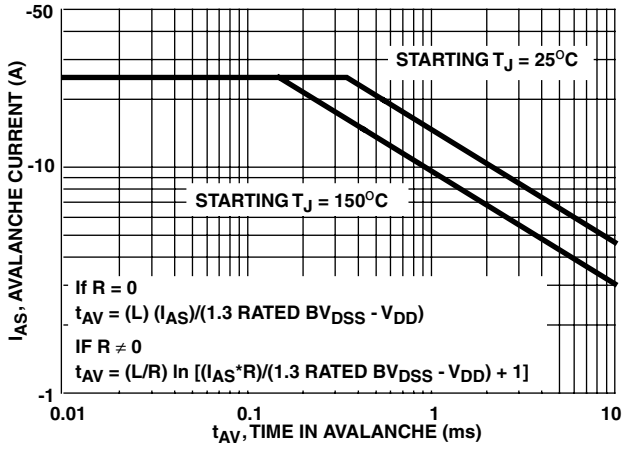


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

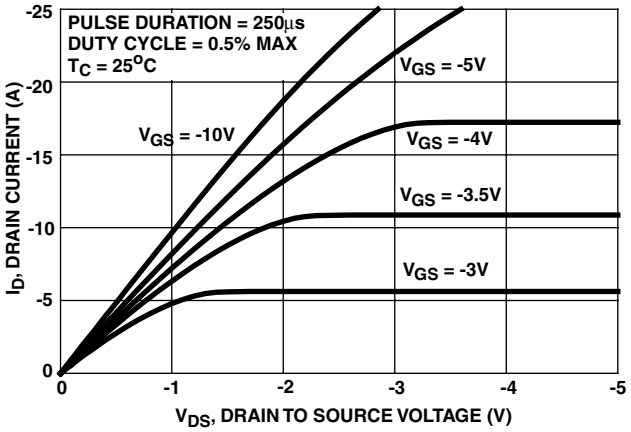


FIGURE 7. SATURATION CHARACTERISTICS

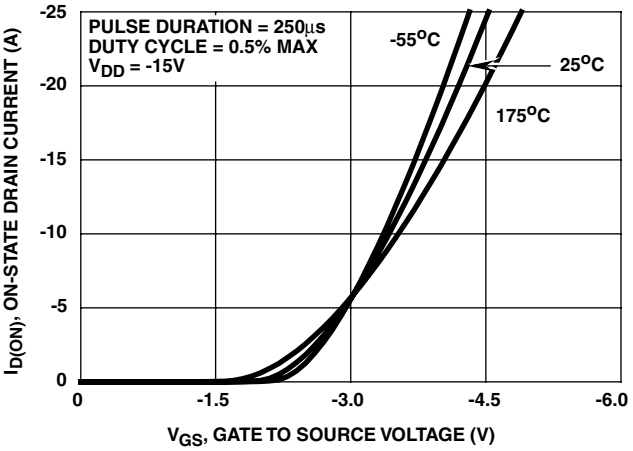


FIGURE 8. TRANSFER CHARACTERISTICS

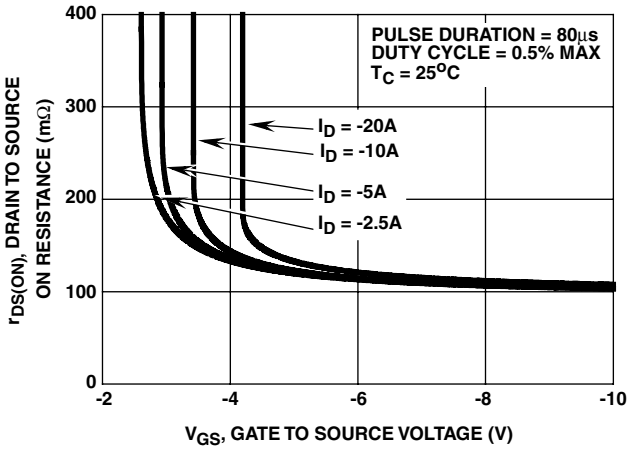


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

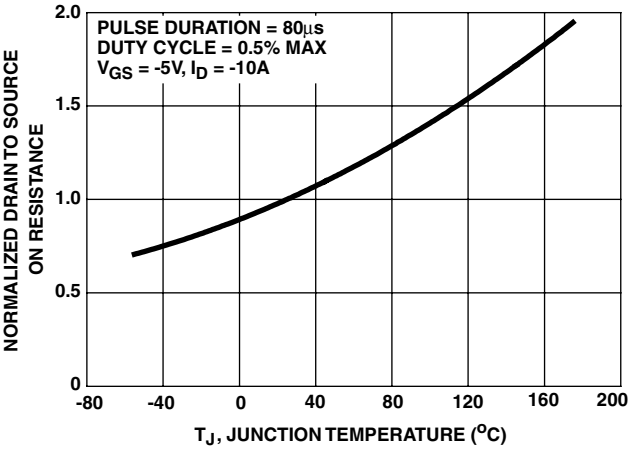


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

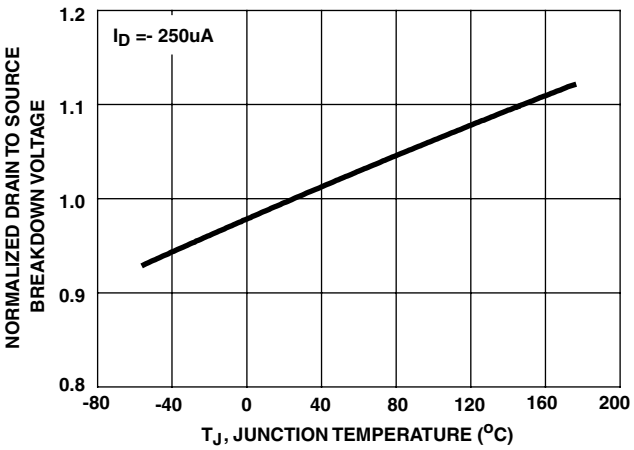


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

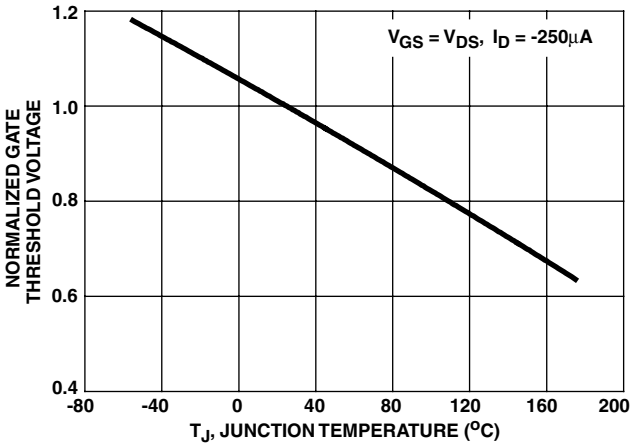


FIGURE 12. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

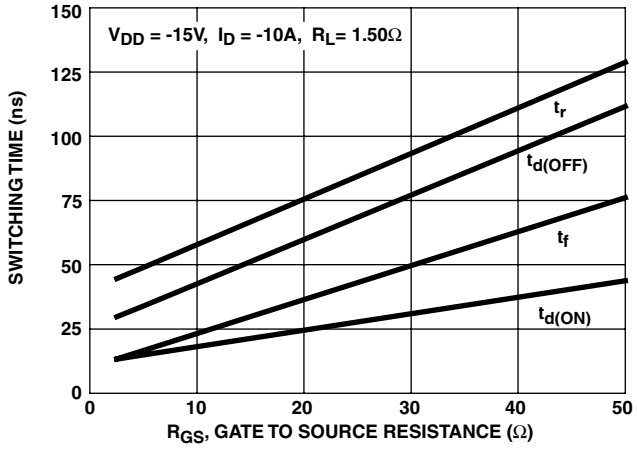
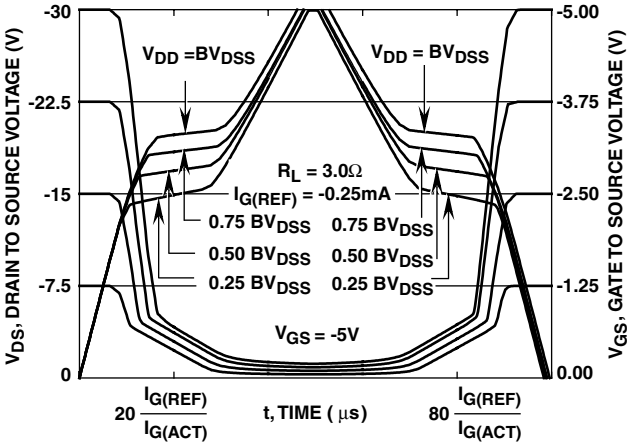


FIGURE 13. SWITCHING TIME vs GATE RESISTANCE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 14. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

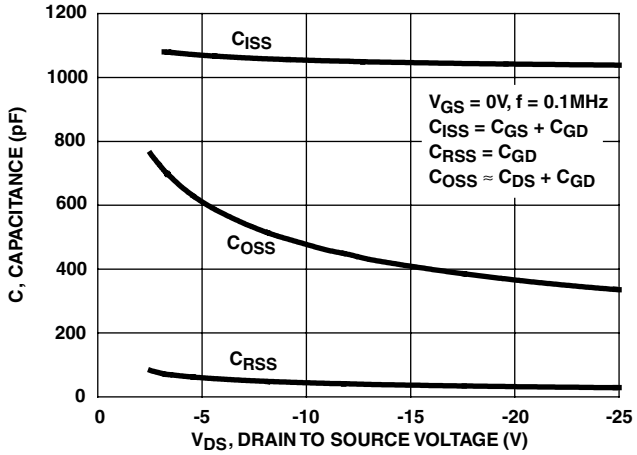


FIGURE 15. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Test Circuits and Waveforms

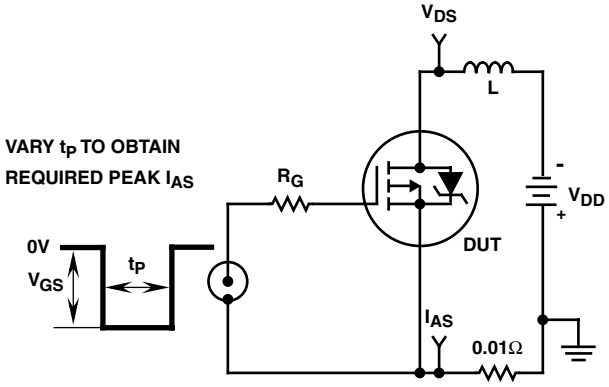


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

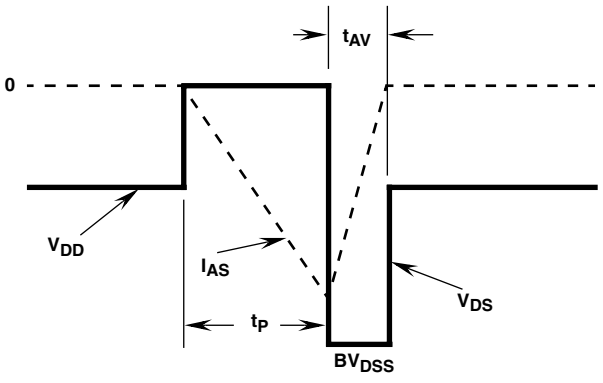


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

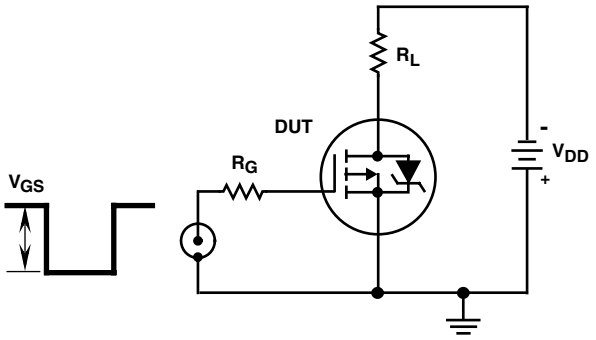


FIGURE 18. SWITCHING TIME TEST CIRCUIT

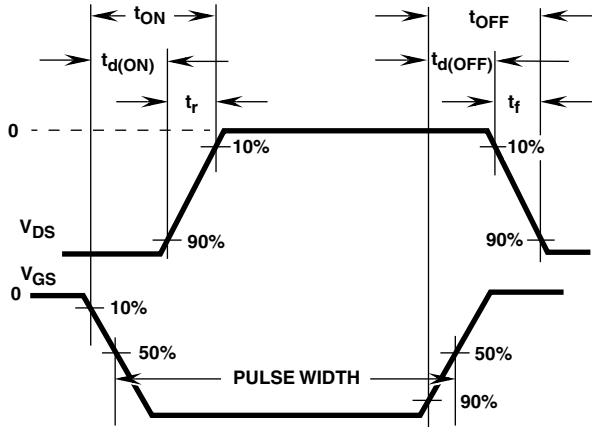


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

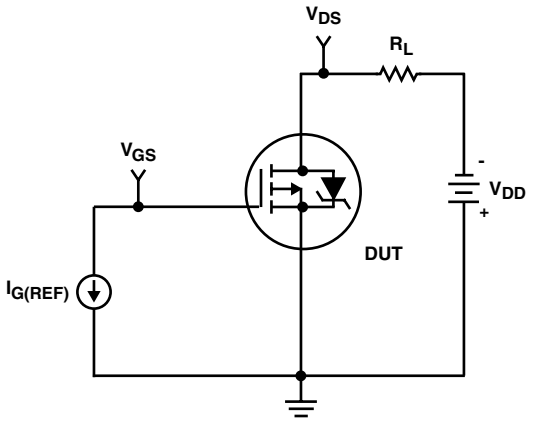


FIGURE 20. GATE CHARGE TEST CIRCUIT

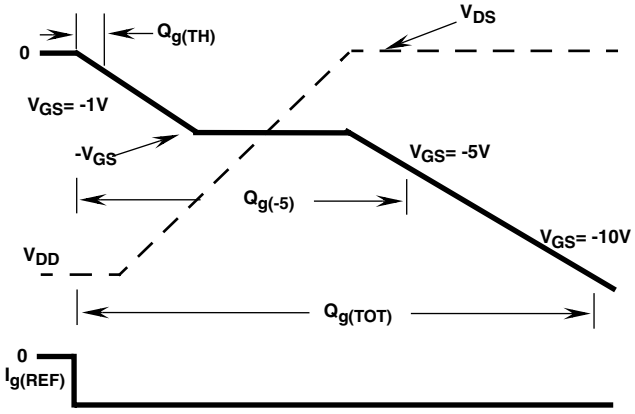


FIGURE 21. GATE CHARGE WAVEFORMS

PSpice Electrical Model

.SUBCKT RFD10P03L 2 1 3 REV 22 Aug 96

CA 12 8 1.29e-9
CB 15 14 9.90e-10
CIN 6 8 1.01e-9

DBODY 5 7 DBODYMOD
DBREAK 7 11 DBREAKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -36.49
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTHRES 6 21 19 8 1
EVTEMP 6 20 18 22 1

IT 8 17 1

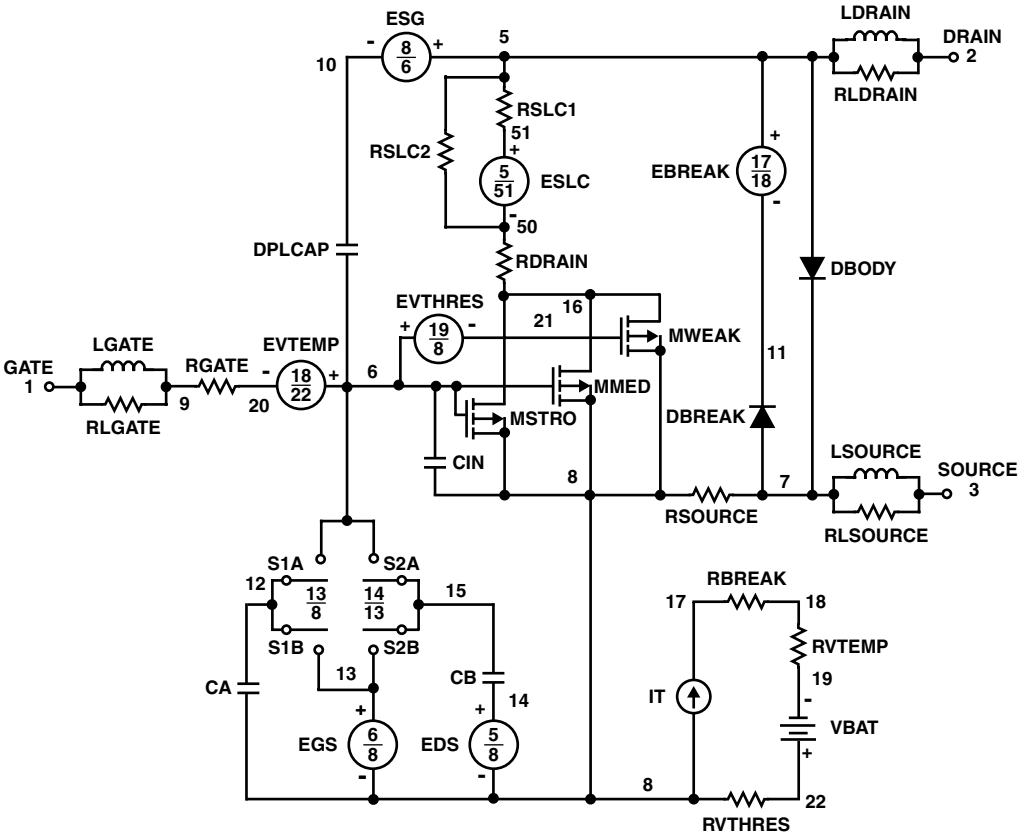
LDRAIN 2 5 1e-9
LGATE 1 9 3.40e-9
LSOURCE 3 7 3.22e-9

MMED 16 6 8 8 MmedMOD
MSTRO 16 6 8 8 MstroMOD
MWEAK 16 21 8 8 MweakMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 68.25e-3
RGATE 9 20 2.54
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RSourceMOD 25.00e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1



ESCL 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*33),5.0))}

.MODEL DBODYMOD D (IS=9.15e-13 RS=3.25e-2 IKF=0.05 N=0.97 TRS1=4.11e-5 TRS2=2.03e-6 CJO=1.13e-9 M=0.40 TT=3.72e-8)
.MODEL DBREAKMOD D (RS=2.62e-1 TRS1=1.74e-3 TRS2=-3.81e-6)
.MODEL DPLCAPMOD D (CJO=1.46e-10 IS=1e-30 N=10 M=0.50)
.MODEL MSTRONGMOD PMOS (VTO=-1.95 KP=11.60 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL MMEDMOD PMOS (VTO=-1.65 KP=1.00 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=2.54)
.MODEL MWEAKMOD PMOS (VTO=-1.43 KP=0.09 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=25.4 RS=0.1)
.MODEL RBREAKMOD RES (TC1=9.17e-4 TC2=-2.74e-7)
.MODEL RDRAINMOD RES (TC1=6.35e-3 TC2=1.98e-5)
.MODEL RSOURCEMOD RES (TC1=0 TC2=0)
.MODEL RSCLMOD RES (TC1=2e-3 TC2=0)
.MODEL RVTHRESMOD RES (TC1=1.23e-3 TC2=1.97e-6)
.MODEL RVTEMPMOD RES (TC1=-1.18e-3 TC2=1.44e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=4.80 VOFF=1.80)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1.80 VOFF=4.80)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.40 VOFF=-3.40)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.40 VOFF=-0.40)
ENDS

For further discussion of the PSPICE model consult A New PSPICE Sub-circuit for the Power MOSFet Featuring Global Temperature Options; authored by William J. Hepp and C. Frank Wheatley.

PSpice Thermal Model

REV 29 Aug 96

RFP10P03L

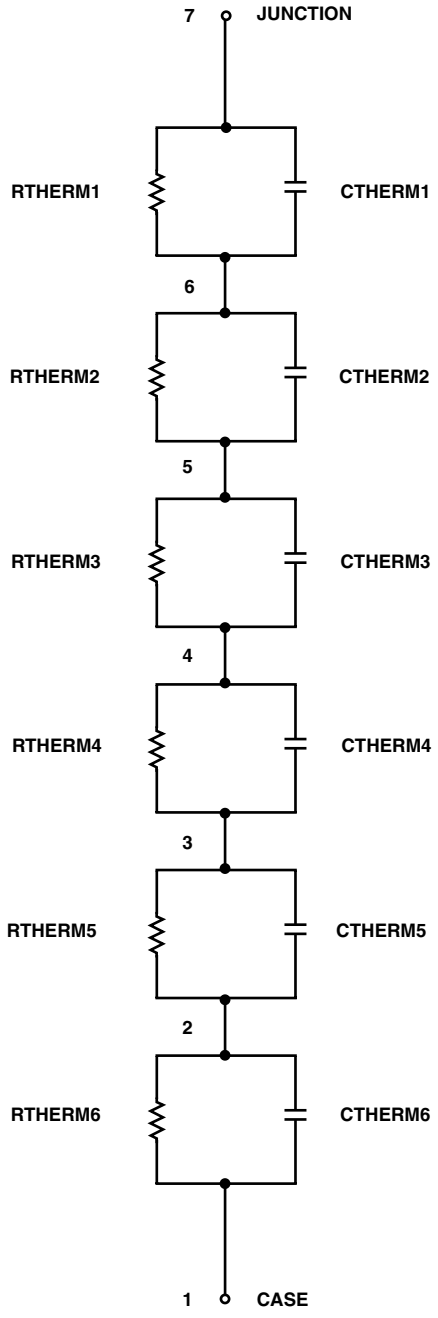
CTHERM1 7 6 5.00e-7
CTHERM2 6 5 5.35e-4
CTHERM3 5 4 5.50e-4
CTHERM4 4 3 1.75e-3
CTHERM5 3 2 1.25e-2
CTHERM6 2 1 0.45

RTHERM1 7 6 1.00e-2
RTHERM2 6 5 2.05e-2
RTHERM3 5 4 5.39e-2
RTHERM4 4 3 5.45e-1
RTHERM5 3 2 1.01
RTHERM6 2 1 0.50

RFD10P03L, RFD10P03LSM

CTHERM1 7 6 5.00e-7
CTHERM2 6 5 5.35e-4
CTHERM3 5 4 5.50e-4
CTHERM4 4 3 1.75e-3
CTHERM5 3 2 1.25e-2
CTHERM6 2 1 0.11

RTHERM1 7 6 1.00e-2
RTHERM2 6 5 2.05e-2
RTHERM3 5 4 5.39e-2
RTHERM4 4 3 5.45e-1
RTHERM5 3 2 1.01
RTHERM6 2 1 0.50



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CoolFET™	FRFET™	PACMAN™	Stealth™	
CROSSVOLT™	GlobalOptoisolator™	POP™	SuperSOT™-3	
DenseTrench™	GTO™	Power247™	SuperSOT™-6	
DOME™	HiSeC™	PowerTrench®	SuperSOT™-8	
EcoSPARK™	ISOPLANAR™	QFET™	SyncFET™	
E^2CMOS™	LittleFET™	QS™	TinyLogic™	
EnSigna™	MicroFET™	QT Optoelectronics™	TruTranslation™	
FACT™	MicroPak™	Quiet Series™	UHC™	
FACT Quiet Series™	MICROWIRE™	SILENT SWITCHER®	UltraFET®	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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